



## Features

- ESD Protection for 1 Line with Bi-directional
- Provide ESD protection for the protected line to IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 10\text{kV}$  (contact)
- **Ultra low capacitance: 0.4pF typical**
- Suitable for, **17V and below**, operating voltage applications
- **0402 small DFN package** saves board space
- Protect one I/O line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**
- **AEC-Q101 qualified**

## Applications

- Near Field Communication (NFC)
- RF Signal ESD Protection
- PA ESD Protection
- Antenna ESD Protection
- Hand Held Portable Applications
- Automotive Application

## Description

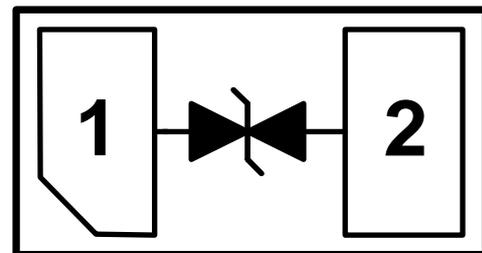
AZ9817-01F is a design which includes a bi-directional ESD rated clamping cell to protect high speed data interfaces in an electronic systems. The AZ9817-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

AZ9817-01F is a unique design which includes proprietary clamping cells with ultra low capacitance in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data lines, protecting any downstream components.

AZ9817-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ9817-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration



**DFN1006P2E (Bottom View)**



## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Operating DC Voltage (I/O to GND)	$V_{DC}$	±18	V
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	±15	kV
ESD per IEC 61000-4-2 (Contact)		±10	kV
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	°C
Operating Temperature	$T_{OP}$	-40 to +125	°C
Storage Temperature	$T_{STO}$	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	$V_{RWM}$	$T = 25\text{ }^{\circ}\text{C}$ , pin-1 to pin-2, or pin-2 to pin-1.	-17		17	V
Reverse Leakage Current	$I_{Leak}$	$V_{RWM} = \pm 17\text{V}$ , $T = 25\text{ }^{\circ}\text{C}$ , pin-1 to pin-2, or pin-2 to pin-1.			1	μA
Reverse Breakdown Voltage	$V_{BV}$	$I_{BV} = 1\text{mA}$ , $T = 25\text{ }^{\circ}\text{C}$ , pin-1 to pin-2, or pin-2 to pin-1.	18.7			V
ESD Clamping Voltage (Note 1)	$V_{clamp}$	IEC 61000-4-2 +8kV ( $I_{TLP} = 16\text{A}$ ), Contact mode, $T = 25\text{ }^{\circ}\text{C}$ , pin-1 to pin-2, or pin-2 to pin-1.		38		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	EC 61000-4-2 0~+8kV, $T = 25\text{ }^{\circ}\text{C}$ , Contact mode, pin-1 to pin-2, or pin-2 to pin-1.		1.0		Ω
Channel Input Capacitance	$C_{IN}$	$V_R = 0\text{V}$ , $f = 1\text{MHz}$ , $T = 25\text{ }^{\circ}\text{C}$ , pin-1 to pin-2.		0.4	0.6	pF

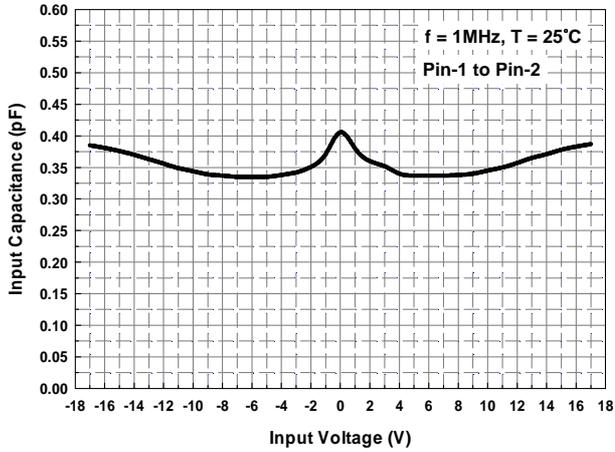
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0 = 50\Omega$ ,  $t_p = 100\text{ns}$ ,  $t_r = 1\text{ns}$ .

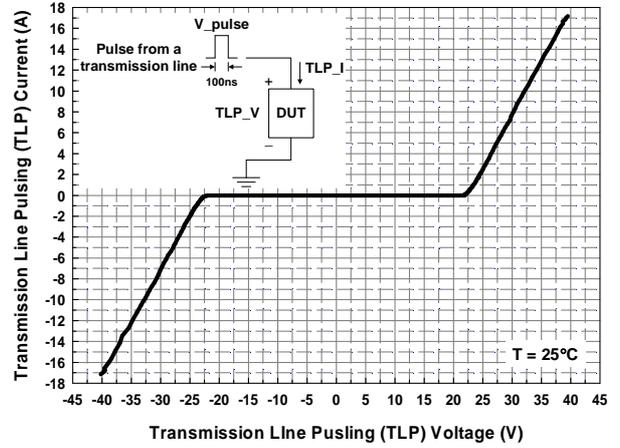


## Typical Characteristics

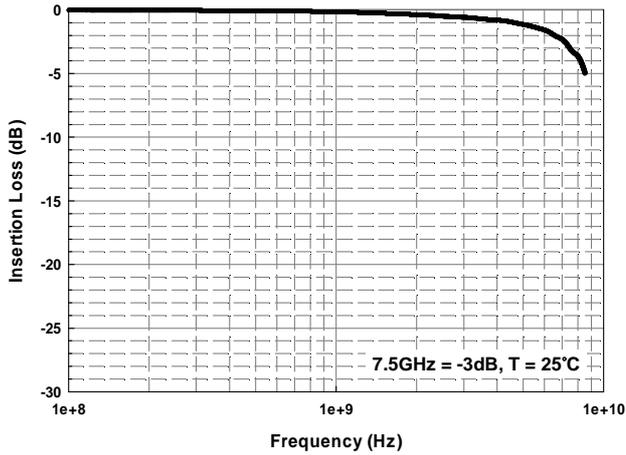
Typical Variation of  $C_{IN}$  vs.  $V_{IN}$



Transmission Line Pulsing (TLP) Measurement



Insertion Loss S21 (IO-to-GND)





## Applications Information

The AZ9817-01F is designed to protect one line against System ESD/CDE pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ9817-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9817-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9817-01F.
- Place the AZ9817-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

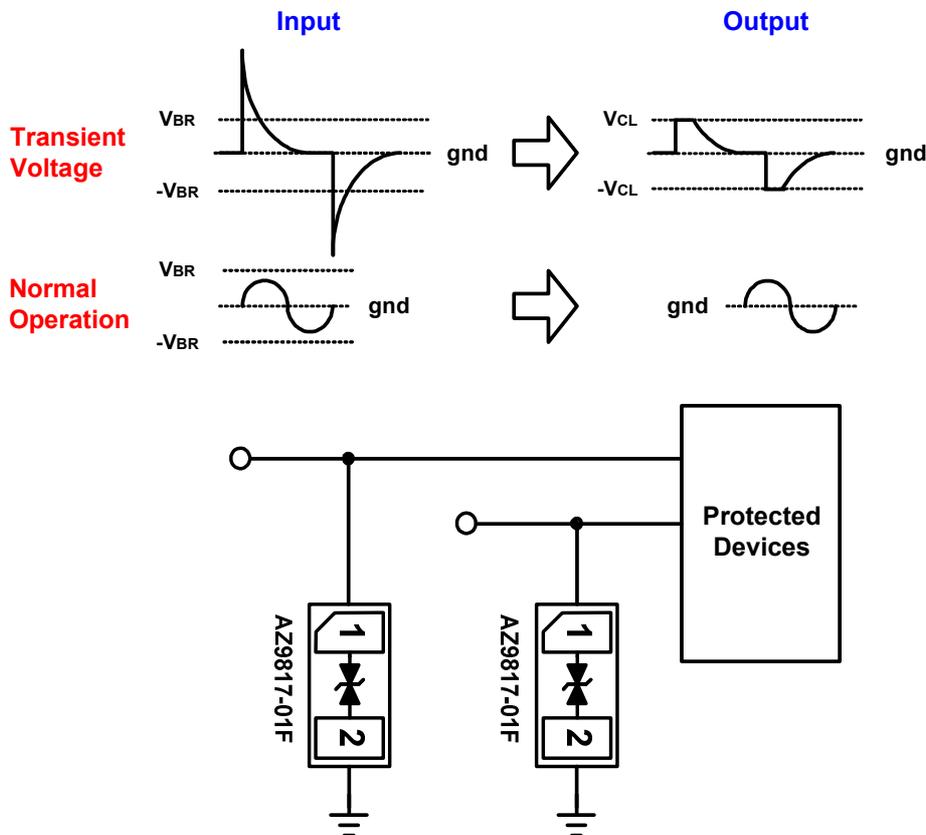
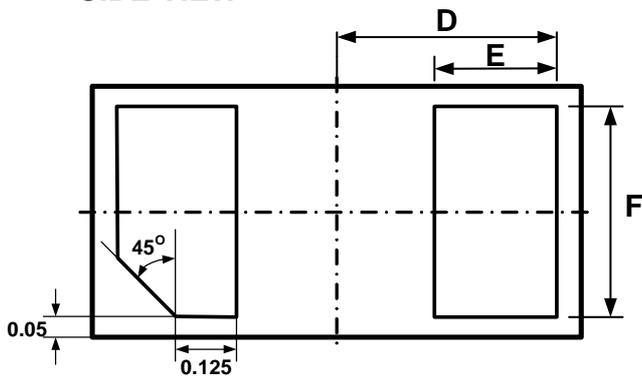
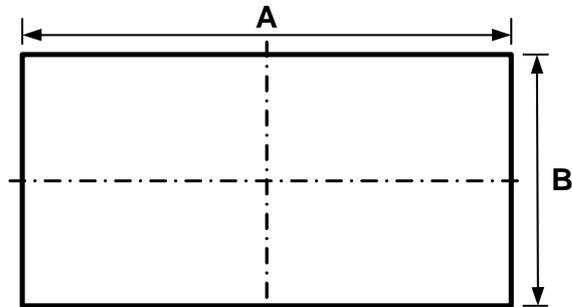


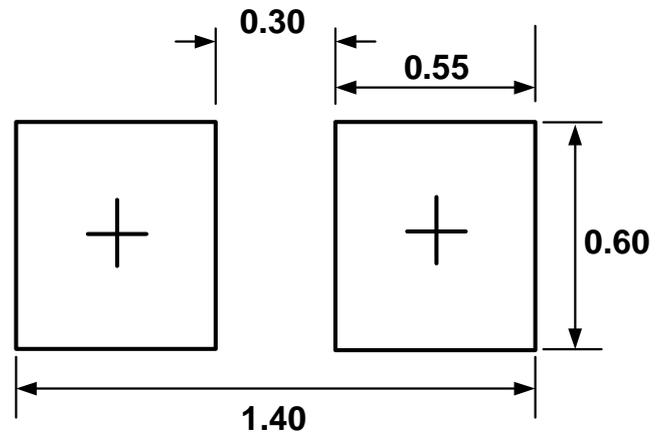
Fig. 1 ESD protection scheme by using AZ9817-01F.

## Mechanical Details

### DFN1006P2E PACKAGE DIAGRAMS



## LAND LAYOUT

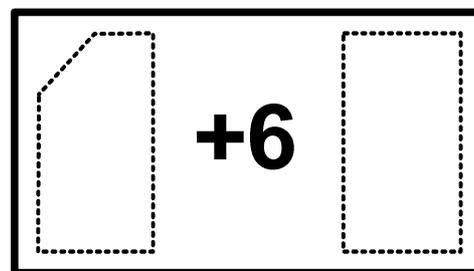


(Unit: mm)

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



Top View

Symbol	Millimeters		Inches	
	min	max	min	max
A	0.95	1.05	0.037	0.041
B	0.55	0.65	0.022	0.026
C	0.45	0.60	0.018	0.024
D	0.45		0.018	
E	0.20	0.30	0.008	0.012
F	0.45	0.55	0.018	0.022

Part Number	Marking Code
AZ9817-01F (Green part)	+6

Note. Green means Pb-free, RoHS, and Halogen free compliant.



### Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9817-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reel = 48,000/box	6 box = 288,000/carton

### Revision History

Revision	Modification Description
Revision 2015/02/06	Preliminary Release.
Revision 2015/10/19	Formal Release.