DID YOU KNOW?

HOW PTCEL ELECTRONIC MODELING HELPS APPLICATION DESIGNS

The PTCEL's definition and dimensioning are crucial parts of a SMPS or battery protection circuit design. The design engineer will have to determine the following points:

- Which PTCEL electrical value must be chosen at ambient temperature?
- How many PTCs must be implemented in parallel, or eventually in series?
- Will the design be efficient at the maximum ambient temperature?

And these are the easy questions; now for the tricky ones:

- Will the application be influenced by the element tolerances?
- How will the voltage-dependent resistor (VDR) effect influence the inrush decay?

For all these questions, prior to the realization of the real board, analog circuit electronic simulation can give the design engineer a low cost helping hand. Whether they use the classical SPICE technique (LTspice® will be a must here), or a multidisciplinary language like VHDL-AMS (here SystemVision® Cloud from Mentor, a Siemens business, is highly recommended www.systemvision.com), there will always be a fast and cheap, but efficient, solution for modeling the application.

To illustrate this, Fig. 1 shows the current and voltage waveforms in an SMPS simulation made on SystemVision® Cloud. The left virtual scope shows how at circuit switch-on, a smoothing capacitance is charging from 0 V to full voltage, draining an important overcurrent that needs to be limited by a two-PTCEL network. After the capacitance charge, switches disconnect the PTC network from the circuit and current is put on the load. On the right pane, the same circuit is working abnormally: the smoothing capacitance is initially shortcircuited. The PTCs switch one after the other, take back all the power supply voltage, and cut all current onto the circuit.

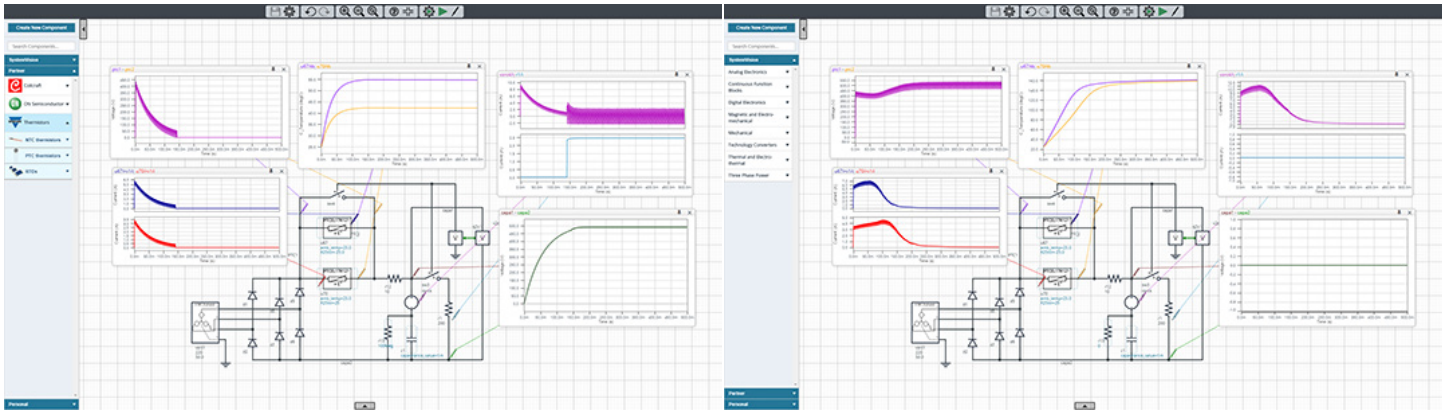

Fig. 1 - Simulation of PTCEL current limiting in an SMPS application (in SystemVision® Cloud)

nlr@vishay.com