

# DRV10974 12-V, Three-Phase, Sensorless BLDC Motor Driver

## 1 Features

- Input Voltage Range: 4.4 V to 18 V
- Total Driver H + L  $r_{DS(on)}$ : 750 m $\Omega$  (Typical) at  $T_A = 25^\circ\text{C}$
- Phase Drive Current: 1-A Continuous (1.5-A Peak)
- 180° Sinusoidal Commutation for Optimal Acoustic Performance
- Resistor-Configurable Lead Angle
- Resistor-Configurable Current Limit
- Soft Start With Resistor-Configurable Acceleration Profile
- Built-In Current Sense to Eliminate External Current-Sense Resistor
- Proprietary Sensorless Control Without Motor Center Tap
- Simple User Interface:
  - One-Pin Configuration for Start-Up
  - PWM Input Designates Magnitude of Voltage Applied to Motor
  - Open-Drain FG Output Provides Speed Feedback
  - Pin for Forward and Reverse Control
- Fully Protected:
  - Motor-Lock Detect and Restart
  - Overcurrent, Short-Circuit, Overtemperature, Undervoltage

## 2 Applications

- White Goods
- Fans, Blowers, and Pumps
- BLDC Motor Module

## 3 Description

The DRV10974 device is a three-phase sensorless motor driver with integrated power MOSFETs, which can provide continuous drive current up to 1 A (rms). The device is designed for cost-sensitive, low-noise, and low-external-component-count applications.

The DRV10974 device uses a proprietary sensorless control scheme to provide dependable commutation. The 180° sinusoidal commutation significantly reduces pure tone acoustics that are typical with 120° (trapezoidal) commutation. The DRV10974 spin-up is configured using a single external low-power resistor. The current limit can be set by an external low-power resistor.

The DRV10974 device provides for simple control of motor speed by applying a PWM input to control the

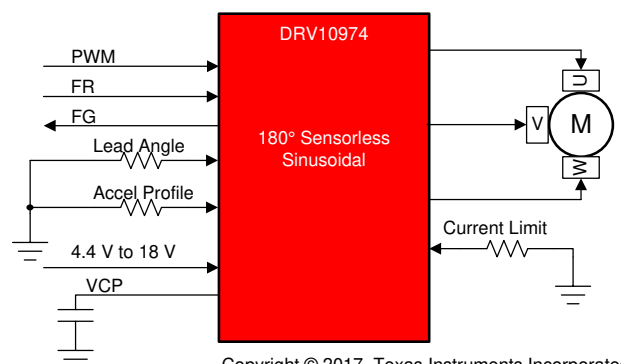
magnitude of the drive voltage, or by driving the PWM pin with an analog voltage and monitoring the FG pin for speed feedback.

The DRV10974 device includes a number of features to improve efficiency. The resistor-configurable lead angle allows the user to optimize the driver efficiency by aligning the phase current and the phase BEMF. In addition, the use of low- $r_{DS(on)}$  MOSFETs helps to conserve power while the motor is being driven.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV10974	HTSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Copyright © 2017, Texas Instruments Incorporated

### Application Schematic



## Table of Contents

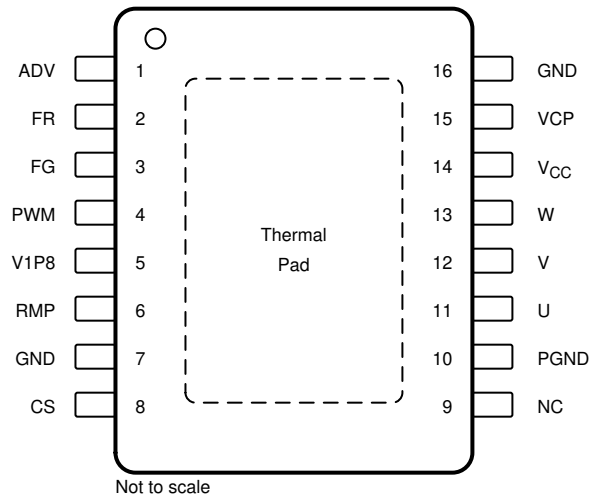
<b>1 Features</b> .....	1	7.4 Device Functional Modes.....	19
<b>2 Applications</b> .....	1	<b>8 Application and Implementation</b> .....	24
<b>3 Description</b> .....	1	8.1 Application Information.....	24
<b>4 Revision History</b> .....	2	8.2 Typical Application.....	24
<b>5 Pin Configuration and Functions</b> .....	3	<b>9 Power Supply Recommendations</b> .....	26
<b>6 Specifications</b> .....	5	<b>10 Layout</b> .....	27
6.1 Absolute Maximum Ratings.....	5	10.1 Layout Guidelines.....	27
6.2 ESD Ratings.....	5	10.2 Layout Example.....	27
6.3 Recommended Operating Conditions.....	5	<b>11 Device and Documentation Support</b> .....	28
6.4 Thermal Information.....	5	11.1 Device Support.....	28
6.5 Electrical Characteristics.....	6	11.2 Receiving Notification of Documentation Updates..	28
6.6 Typical Characteristics.....	10	11.3 Support Resources.....	28
<b>7 Detailed Description</b> .....	11	11.5 Electrostatic Discharge Caution.....	28
7.1 Overview.....	11	11.6 Glossary.....	28
7.2 Functional Block Diagram.....	12	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	28
7.3 Feature Description.....	12		

## 4 Revision History

Changes from Revision D (June 2020) to Revision E (March 2021)	Page
• Updated Human-body model (HBM).....	5
Changes from Revision B (June 2018) to Revision C (September 2018)	Page
• Changed document status from MIXED STATUS to PRODUCTION DATA.....	1
• Deleted "Adv. info." designation from the WQFN entry in the <i>Device Information</i> table.....	1
• Deleted the "Advance informatoin" note from the WQFN pinout drawing.....	3
• Deleted the "Advance Information" note from the <i>Thermal Information</i> table.....	5
• Added description of Analog Mode Speed Control.....	12
• Added Kt High and Kt Low descriptions in abnormal Kt lock detect figure.....	16
• Added layout example for QFN package type.....	27
Changes from Revision A (April 2018) to Revision B (June 2018)	Page
• Added WQFN package to the <i>Device Information</i> table.....	1
• Added pinout drawing for the WQFN package.....	3
• Added a column to the <i>Pin Functions</i> table for the WQFN package, and added the TYPE column.....	3
• Added a column to the <i>Thermal Information</i> table for the VQFN package.....	5
• Changed $r_{DS(on)}$ vs. Temperature graph to include $V_{CC}$ condition.....	10
• Changed Speed-Control Transfer Function figure to clearly show when the device enters and exits low power mode .....	12
• Updated Lock BEMF Abnormal text for clarity.....	16
• Changed <i>Detailed Design Procedure</i> to cover the high level tuning process of the RMP, ADV, and CS settings.....	25
Changes from Revision * (January 2018) to Revision A (April 2018)	Page
• Added or changed several bullets in the <a href="#">Section 1</a> list .....	1
• Changed text in the third paragraph of the <a href="#">Section 3</a> section.....	1
• Added parameter symbol ( $f_{PWM\_OUT}$ ) to the 25-kHz PWM signal.....	12
• Added parameter symbol ( $f_{PWM\_OUT}$ ) to the 25-kHz PWM signal.....	12
• Added parameter symbol ( $DC_{STEP}$ ) for the control resolution.....	12
• Added parameter symbol ( $DC_{ON\_MIN}$ ) for the minimum-operation duty cycle.....	12

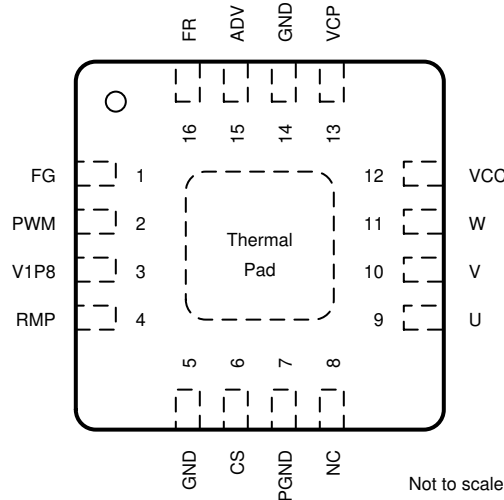
- Changed "pulse durations" to "duty cycles"..... 12
- Changed PWM<sub>DC</sub> to PWM<sub>dc</sub> ..... 12
- Added parameter symbol ( $f_{FG\_MIN}$ ) for the motor speed..... 15
- Changed the number of lock-detect schemes from five to six..... 15
- Added a table note stating the required resistor tolerance..... 18
- Added a new [Section 7.4.1.2](#) section..... 19
- Added a parameter symbol ( $t_{ALIGN}$ ) in the [Section 7.4.1.3](#) section, and reworded the last sentence thereof.. 20
- Changed the column headings of the two rightmost columns in [Table 7-2](#) ..... 20
- Added three table notes following [Table 7-2](#) ..... 20
- Changed "programmed resistor" to "selected resistor"..... 21
- Added a table note stating the required resistor tolerance..... 21
- Added a table note stating the required resistor tolerance..... 22
- Added a  $\pm 30\%$  tolerance to the V1P8 capacitor in [Table 8-1](#) ..... 24
- Changed content of Row 4 in [Table 8-2](#) to "Motor electrical constant"..... 25
- Deleted all previous content from the [Section 8.2.2](#) section and replaced it with a reference to the *DRV10974 Tuning Guide* ..... 25
- Changed [Figure 8-3](#) ..... 25
- Added location information for the capacitor in the [Section 9](#) section..... 26

## 5 Pin Configuration and Functions



NC – No internal connection

**Figure 5-1. PWP PowerPAD™ Package 16-Pin HTSSOP With Exposed Thermal Pad Top View**



NC – No internal connection

**Figure 5-2. RUM Package 16-Pin WQFN With Exposed Thermal Pad Top View**

**Table 5-1. Pin Functions**

NAME.	PIN		I/O	TYPE <sup>(1)</sup>	DESCRIPTION
	HTSSOP	WQFN			
ADV	1	15	I	D	Selects the applied lead angle by 1/8-W resistor; not to be driven externally with a source; leaving the pin open results in the longest lead angle; the lead angle is determined by the ADV pin voltage at power up.
CS	8	6	I	D	Selects current limit by 1/8-W resistor; not to be driven externally with a source; leaving the pin open results in the highest current limit; the current limit is determined by the CS pin voltage at power up.
FG	3	1	O	D	Provides motor speed feedback; open-drain output with internal pullup to V3P3; needs a pullup resistor to limit current if pullup voltage is higher than V3P3
FR	2	16	I	D	Direction control. FR = 0: U→V→W; FR = 1: U→W→V; value is determined by the FR pin state on exit of low-power mode; internal pulldown
GND	7, 16	5, 14	—	—	Digital and analog ground
NC	9	8	—	NC	No internal connection
PGND	10	7	—	P	Power ground connection for motor power
PWM	4	2	I	D	Motor speed-control input; auto detect for analog or digital mode; internal pullup to 2.2 V
RMP	6	4	I	D	Acceleration ramp-rate control; 1/8-W resistor to GND to set acceleration rate; leaving the pin open results in the slowest acceleration rate; the acceleration rate is determined by the RMP pin voltage at power up.
U	11	9	I/O	A	Motor phase U
V	12	10	I/O	A	Motor phase V
V1P8	5	3	O	P	LDO regulator for internal operation; 1-μF, 6.3-V ceramic capacitor tied to GND. Can supply a maximum of 3 mA to an external load.
V <sub>CC</sub>	14	12	I	P	Power-supply connection; 10-μF, 25-V ceramic capacitor tied to GND
VCP	15	13	O	A	Charge-pump output; 100-nF, 10-V ceramic capacitor tied to V <sub>CC</sub>
W	13	11	I/O	A	Motor phase W
Thermal pad	—	—	—	—	The exposed thermal pad must be electrically connected to the ground plane by soldering to the PCB for proper operation, and connected to the bottom side of the PCB through vias for better thermal spreading.

(1) I = Input, O = Output, I/O = Input/output, P = Power, D = Digital, A = Analog, NC = No connection

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage	V <sub>CC</sub>	-0.3	20	V
	PWM, FR	-0.3	5.5	
	CS, RMP, ADV	-0.3	2	
	GND, PGND	-0.3	0.3	
	U, V, W	-1	20	
	V1P8	-0.3	2	
	FG	-0.3	20	
	VCP	-0.3	V <sub>CC</sub> + 5.5	
Maximum junction temperature, T <sub>Jmax</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V <sub>CC</sub>	4.4		18	V
Voltage	U, V, W	-0.7		18	V
	PWM, FR	-0.1		5.5	
	FG	0.5		18	
	CS	-0.1		1.8	
	PGND, GND	-0.1		0.1	
	RMP, ADV	-0.1		1.8	
Current	V1P8 regulator-output current; external load	0		3	mA
Operating ambient temperature, T <sub>A</sub>		-40		85	°C
Operating junction temperature, T <sub>J</sub>		-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DRV10974		UNIT
		PWP (HTSSOP)	RUM (VQFN)	
		16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	37.8	34.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	25.2	27	°C/W

THERMAL METRIC <sup>(1)</sup>		DRV10974		UNIT
		PWP (HTSSOP)	RUM (VQFN)	
		16 PINS	16 PINS	
R <sub>θJB</sub>	Junction-to-board thermal resistance	20.7	13.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	20.5	13.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	1.9	4	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>CC</sub>	Supply current	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 12 V, no motor load		5	7	mA
I <sub>CC(LP)</sub>	Low power mode	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 12 V		380		µA
<b>UVLO</b>						
V <sub>(UVLO_F)</sub>	V <sub>CC</sub> UVLO falling		4.2	4.3	4.4	V
V <sub>(UVLO_R)</sub>	V <sub>CC</sub> UVLO rising		4.5	4.7	4.85	V
V <sub>hys(UVLO)</sub>	V <sub>CC</sub> UVLO hysteresis			400		mV
V <sub>VCP(UVLO_F)</sub>	Charge pump UVLO falling	V <sub>VCP</sub> – V <sub>CC</sub>	3.35	3.7	4.05	V
V <sub>VCP(UVLO_R)</sub>	Charge pump UVLO rising	V <sub>VCP</sub> – V <sub>CC</sub>	3.65	4.0	4.37	V
V <sub>hys(VCP)</sub>	Charge pump UVLO hysteresis			330		mV
V <sub>(V1P8_F)</sub>	V1P8 UVLO falling		1.25	1.4	1.55	V
V <sub>(V1P8_R)</sub>	V1P8 UVLO rising		1.35	1.5	1.65	V
V <sub>hys(V1P8)</sub>	V1P8 UVLO hysteresis			100		mV
<b>VOLTAGE REGULATORS</b>						
V <sub>V1P8</sub>	V1P8 voltage	T <sub>A</sub> = 25°C, C <sub>(V1P8)</sub> = 1 µF	1.7	1.8	1.9	V
I <sub>V1P8</sub>	Maximum external load from V1P8	T <sub>A</sub> = 25°C, C <sub>(V1P8)</sub> = 1 µF			3	mA
<b>INTEGRATED MOSFET</b>						
r <sub>ds(on)_HS</sub>	High-side FET on-resistance	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 12 V, I <sub>O</sub> = 100 mA		0.375	0.425	Ω
r <sub>ds(on)_LS</sub>	Low-side FET on-resistance	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 12 V, I <sub>O</sub> = 100 mA		0.375	0.425	Ω
<b>PHASE DRIVER</b>						
SL <sub>PH_LH</sub>	Phase slew rate switching low to high	SlewRate = 0; measure 20% to 80%; V <sub>CC</sub> = 12 V; phase current > 20 mA	70	120	170	V/µs
SL <sub>PH_HL</sub>	Phase slew rate switching high to low	SlewRate = 0; measure 80% to 20%; V <sub>CC</sub> = 12 V; phase current > 20 mA	70	120	170	V/µs
f <sub>PWM_OUT</sub>	Phase output PWM frequency			25		kHz
t <sub>dead_time</sub>	Recommended dead time		440			ns
<b>CHARGE PUMP</b>						
V <sub>VCP</sub>	VCP voltage	V <sub>CC</sub> = 4.4 V to 18 V	V <sub>CC</sub> + 4	V <sub>CC</sub> + 5	V <sub>CC</sub> + 5.5	V
<b>CURRENT LIMIT</b>						

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>LIMIT</sub>	Current-limit threshold	V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 7.32 kΩ ±1%		0.2		A
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 16.2 kΩ ±1%		0.4		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 25.5 kΩ ±1%		0.6		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 38.3 kΩ ±1%		0.8		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 54.9 kΩ ±1%		1		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 80.6 kΩ ±1%		1.2		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 115 kΩ ±1%		1.4		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 182 kΩ ±1%, open loop and closed loop current limit		1.6		
		V <sub>CC</sub> = 12 V, R <sub>(CS)</sub> = 182 kΩ ±1%, align current limit		1.5		
<b>RANGE OF MOTORS SUPPORTED</b>						
R <sub>m</sub>	Motor resistance measurement	Phase to center tap	1		20	Ω
K <sub>t</sub>	Motor BEMF constant measurement	Phase to center tap	5		150	mV/Hz
t <sub>ALIGN</sub>	Motor align time			0.67		s

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>PWM - DIGITAL MODE</b>						
$V_{IH(DIG)}$	PWM input high voltage		2.2			V
$V_{IL(DIG)}$	PWM input low voltage				0.6	V
$f_{PWM}$	PWM input frequency		0.1		100	kHz
$DC_{MAX}$	Maximum output PWM duty cycle	$V_{VCC} < 14\text{ V}$	100 %			
		$V_{VCC} \geq 14\text{ V}$	[(14 / $V_{VCC}$ ) × 100] %			
$DC_{MIN}$	Minimum output PWM duty cycle device needs to guarantee (irrespective of input PWM DC)	Lower duty cycle from 15% down	15%			
$DC_{ON\_MIN}$	Minimum input duty cycle that device uses to drive motor		1.5 %			
$DC_{STEP}$	Duty cycle step size/resolution		0.2 %			
$V_{IH(AUTO)}$	PWM input high voltage for auto detection		1.62	1.695	1.77	V
$V_{IL(AUTO)}$	PWM input low voltage for exiting PWM mode		1.315	1.39	1.465	V
$R_{pu(PWM)}$	Internal PWM pullup resistor to V3P3		120			k $\Omega$
<b>LOW-POWER MODE</b>						
$t_{EX\_LPM}$	PWM pulse duration to exit low-power mode	$PWM > V_{IH(DIG)}$	1			$\mu\text{s}$
$V_{EX\_LPM}$	PWM voltage to exit low-power mode		1.5			V
$t_{EN\_LPM}$	PWM low time to enter low-power mode	$PWM < V_{IL(DIG)}$ , motor stationary	25			ms
<b>PWM - ANALOG MODE</b>						
$V_{ANA\_FS}$	Analog full-speed voltage		1.8			V
$V_{ANA\_ZS}$	Analog zero-speed voltage		20			mV
$R_{out(PWM)}$	External analog driver output impedance				50	k $\Omega$
$t_{SAM}$	Analog speed sample period		320			$\mu\text{s}$
$V_{ANA\_RES}$	Analog voltage resolution		3.5			mV
<b>DIGITAL I/O (FG OUTPUT, FR INPUT)</b>						
$f_{FG\_MIN}$	Minimum FG output frequency during coast		10			Hz
$V_{IH(FR)}$	Input high		2.2			V
$V_{IL(FR)}$	Input low				0.6	V
$I_{(FG\_SINK)}$	Output sink current, FG	$V_O = 0.3\text{ V}$	5			mA
$R_{pu(FG)}$	Internal FG pullup resistor to 3.3V		20			k $\Omega$
$R_{pd(FR)}$	Internal FR pulldown resistor to ground		100			k $\Omega$
<b>LOCK DETECTION RELEASE TIME</b>						
$t_{(LOCK\_OFF)}$	Lock release time		5			s
<b>OVERCURRENT PROTECTION</b>						
$I_{OC\_limit}$	Overcurrent protection	$T_A = 25^\circ\text{C}$	2.5			A
$t_{OC\_retry}$	Overcurrent protection retry time		5			s
<b>THERMAL SHUTDOWN</b>						
$T_{SD}$	Shutdown temperature threshold		140	150		$^\circ\text{C}$
$T_{SD(hys)}$	Shutdown temperature threshold hysteresis		15			$^\circ\text{C}$



over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LEAD ANGLE</b>						
ADV <sub>select</sub>	Lead angle selection	V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 10.7 kΩ ±1%		10		μs
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 14.3 kΩ ±1%		25		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 17.8 kΩ ±1%		50		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 22.1 kΩ ±1%		100		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 28 kΩ ±1%		150		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 34 kΩ ±1%		200		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 41.2 kΩ ±1%		250		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 49.9 kΩ ±1%		300		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 59 kΩ ±1%		400		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 71.5 kΩ ±1%		500		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 86.6 kΩ ±1%		600		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 105 kΩ ±1%		700		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 124 kΩ ±1%		800		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 150 kΩ ±1%		900		
		V <sub>CC</sub> = 12 V, R <sub>(ADV)</sub> = 182 kΩ ±1%		1000		
<b>ACCELERATION RAMP RATE</b>						
RMP <sub>select</sub>	RMP selection for acceleration profile	V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 7.32 kΩ ±1%		0		code
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 10.7 kΩ ±1%		1		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 14.3 kΩ ±1%		2		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 17.8 kΩ ±1%		3		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 22.1 kΩ ±1%		4		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 28 kΩ ±1%		5		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 34 kΩ ±1%		6		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 41.2 kΩ ±1%		7		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 49.9 kΩ ±1%		8		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 59 kΩ ±1%		9		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 71.5 kΩ ±1%		10		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 86.6 kΩ ±1%		11		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 105 kΩ ±1%		12		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 124 kΩ ±1%		13		
		V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 150 kΩ ±1%		14		
V <sub>CC</sub> = 12 V, R <sub>(RMP)</sub> = 182 kΩ ±1%		15				

### 6.6 Typical Characteristics

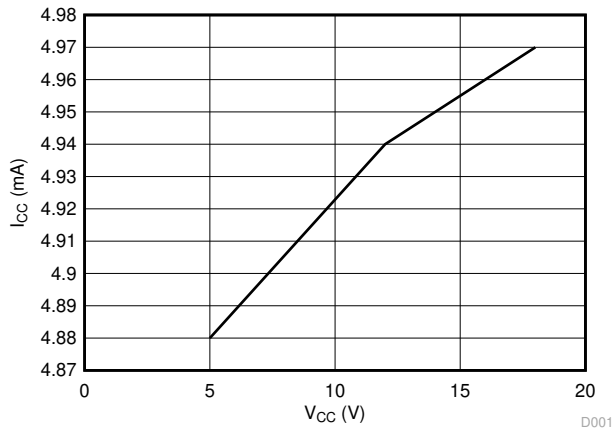
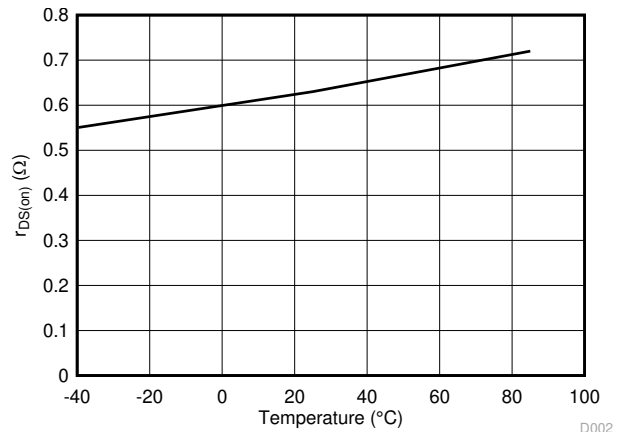


Figure 6-1. Supply Current vs Power Supply



$V_{CC} = 12 V$

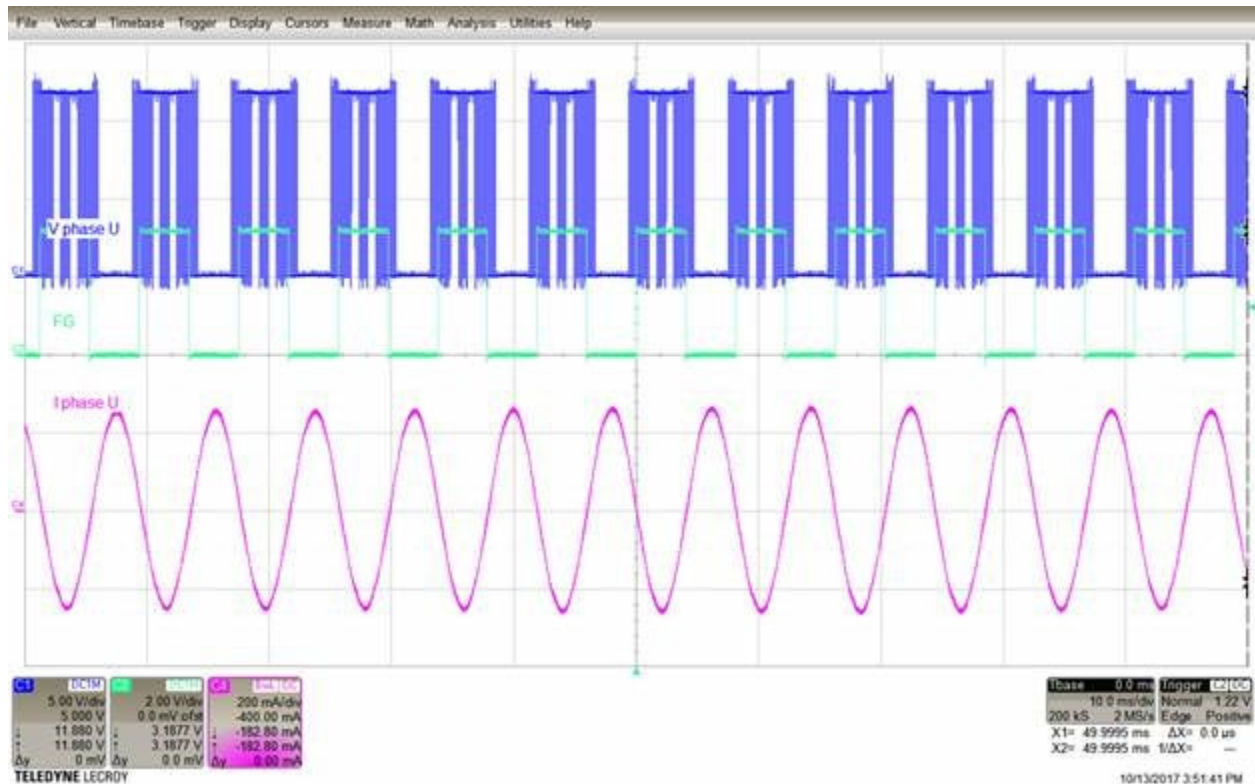
Figure 6-2.  $r_{DS(on)}$  vs Temperature When  $V_{CC} = 12 V$

## 7 Detailed Description

### 7.1 Overview

The DRV10974 device is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive-current capability up to 1 A continuous (rms). The device is specifically designed for low-noise, low external-component count, 12-V motor-drive applications. The 180° commutation requires no configuration beyond setting the peak current, the lead angle, and the acceleration profile, each of which is configured by an external resistor.

The 180° sensorless-control scheme provides sinusoidal output voltages to the motor phases as shown in Figure 7-1.

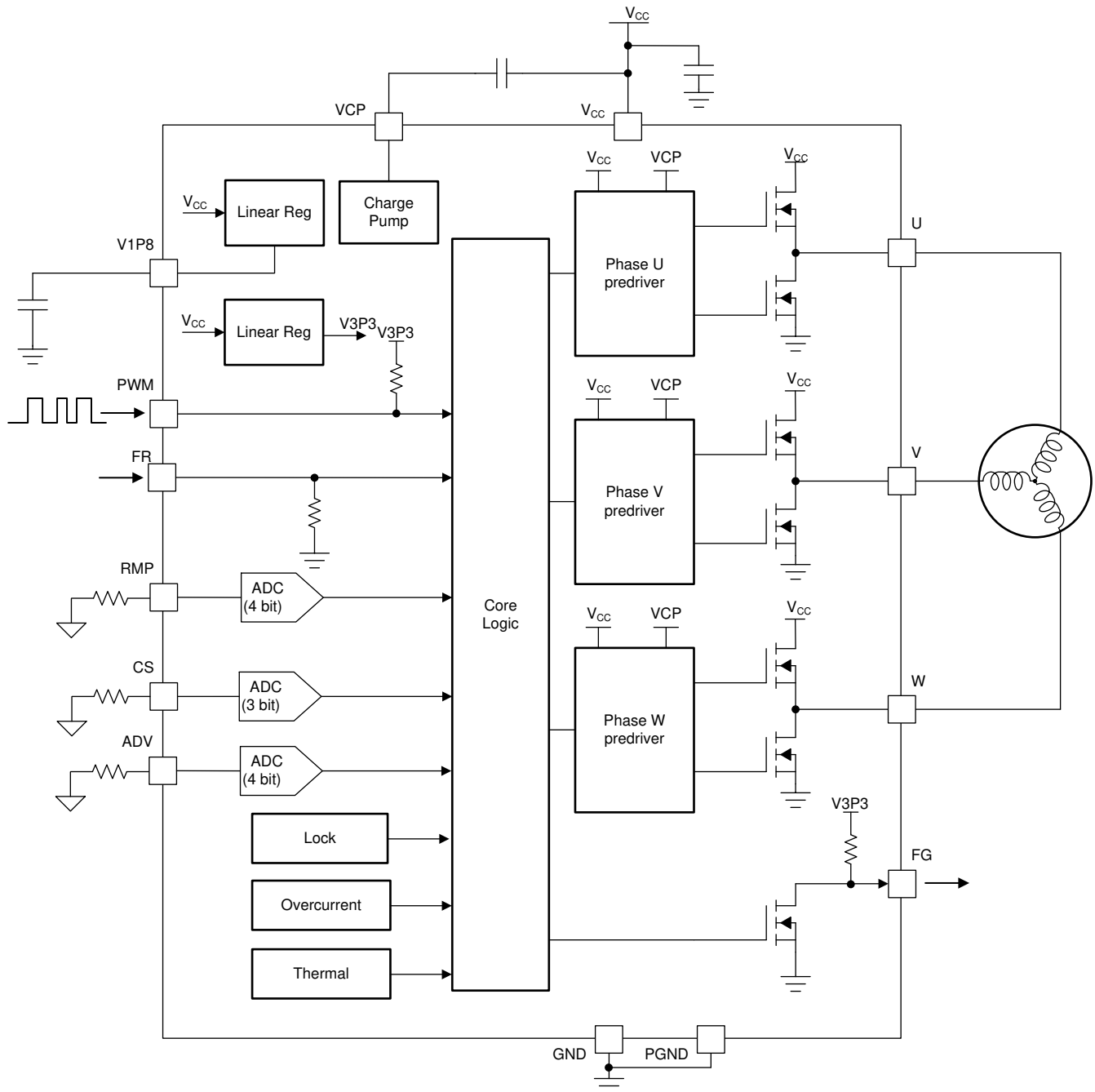


**Figure 7-1. 180° Sensorless-Control Scheme**

Interfacing to the DRV10974 device is simple and intuitive. The DRV10974 device receives a PWM input that it uses to control the speed of the motor. The duty cycle of the PWM input is used to determine the magnitude of the voltage applied to the motor. The resulting motor speed can be monitored on the FG pin. The FR pin is used to control the direction of rotation for the motor. The acceleration ramp rate is controlled by the RMP pin. The current limit is controlled by a resistor on the CS pin. The lead angle is controlled by a resistor on the ADV pin. When the motor is not spinning, a low-power mode turns off unused circuits to conserve power.

The DRV10974 device features extensive protection and fault-detect mechanisms to ensure reliable operation. The device provides overcurrent protection without the requirement for an external current-sense resistor. Rotor-lock detect uses several methods to reliably determine when the rotor stops spinning unexpectedly. The device provides additional protection for undervoltage lockout (UVLO), for thermal shutdown, and for phase short circuit (phase to phase, phase to ground, phase to supply).

## 7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 Speed Input and Control

The DRV10974 device has a three-phase 25-kHz PWM ( $f_{PWM\_OUT}$ ) output that has an average value of sinusoidal waveforms from phase to phase as shown in Figure 7-2. When any phase is measured with reference to ground, the waveform observed is a PWM-encoded sinusoid coupled with third-order harmonics as shown in Figure 7-3. This encoding scheme simplifies the driver requirements because one phase output is always equal to zero.

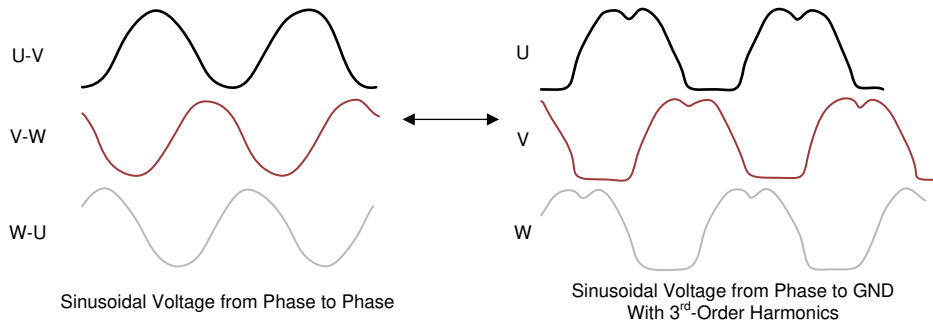


Figure 7-2. Sinusoidal Voltage

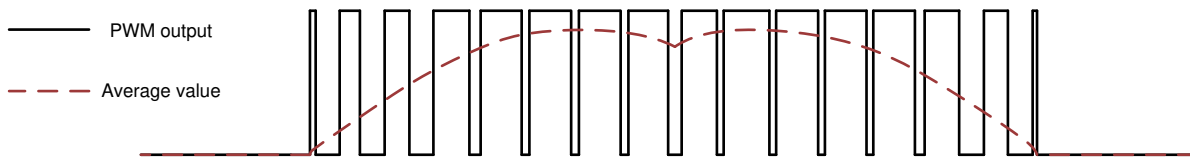


Figure 7-3. PWM Encoded Phase Output and the Average Value

The output amplitude is determined by the supply voltage ( $V_{CC}$ ) and the PWM-commanded duty cycle (PWM) as calculated in Equation 1 and shown in Figure 7-4. The maximum amplitude is applied when the commanded PWM duty cycle is slightly less than 100% in order to keep the 25-kHz PWM rate ( $f_{PWM\_OUT}$ ).

$$V_{ph_{pk}} = PWM_{dc} \times V_{CC} \quad (1)$$

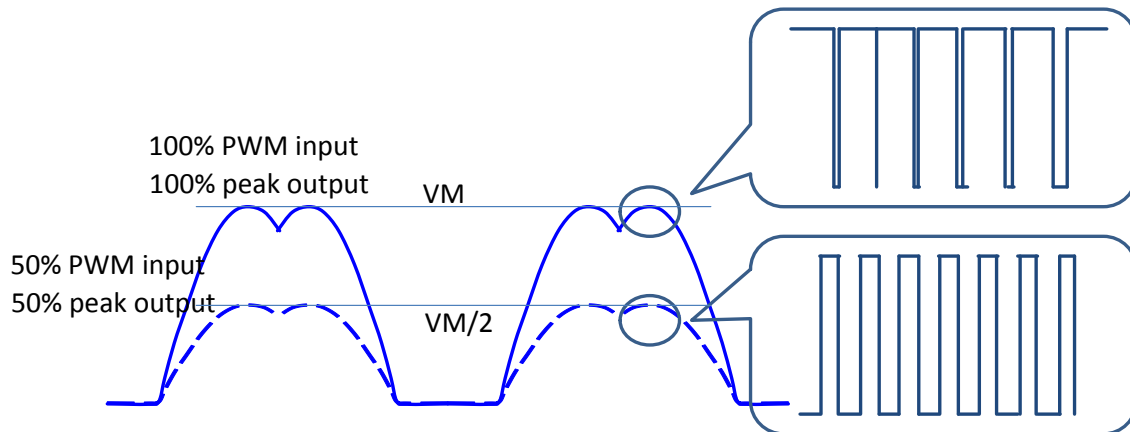


Figure 7-4. Output Voltage Amplitude Adjustment

The motor speed is controlled indirectly by using the PWM command to control the amplitude of the phase voltages which are applied to the motor. The PWM pin can be driven by either a digital duty cycle or an analog voltage.

The duty cycle of the PWM input (PWM) is passed through a low-pass filter that ramps from 0% to 100% duty cycle in 120 ms. The control resolution is approximately 0.2% ( $DC_{STEP}$ ). The signal path from PWM input to PWM motor is shown in Figure 7-5.

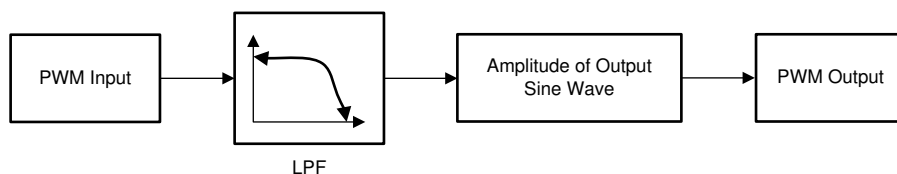
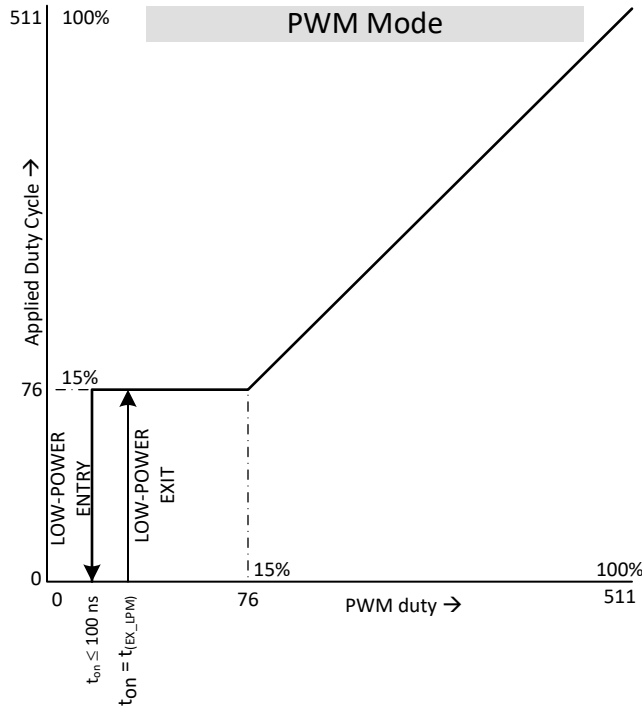


Figure 7-5. PWM Command Input Control Diagram

The output peak amplitude is described by Equation 1 when  $PWM_{dc} > 15\%$  (the minimum-operation duty cycle). When the PWM-commanded duty cycle is lower than the minimum-operation duty cycle and higher than 1.5% ( $DC_{ON\_MIN}$ ), the output is controlled the by the minimum-operation duty cycle ( $DC_{MIN}$ ). This is shown in Figure 7-6 for analog input, and for duty cycles greater than 1.5% ( $DC_{ON\_MIN}$ ) for digital input. If the supply voltage ( $V_{VCC}$ ) > 14 V, the maximum  $PWM_{dc}$  is limited to  $14 V / V_{VCC}$ .



**Figure 7-6. PWM-Mode Speed-Control Transfer Function**

When the PWM pin is driven with an analog voltage, the output peak amplitude depends on the supply voltage, the analog voltage on the PWM pin ( $V_{ANA}$ ), and the voltage of V1P8 ( $V_{V1P8}$ ). This is shown in Equation 2:

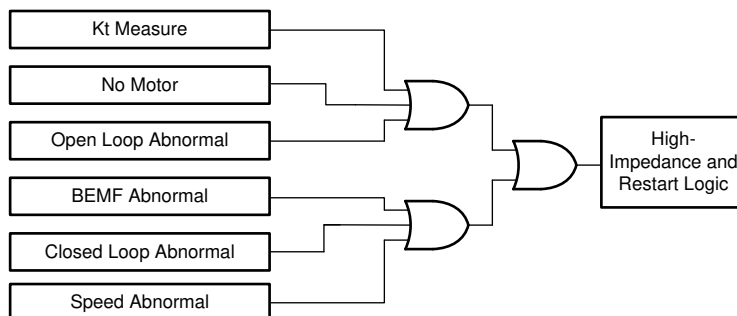
$$V_{ph\_pk} = \frac{V_{ANA}}{V_{1P8}} \times V_{CC} \tag{2}$$

Note the output peak amplitude is described by Equation 2 when the  $V_{ANA} > 0.27 V$  or 15% of 1.8 V. This is the equivalent of the minimum-operation duty cycle percentage of 15% ( $DC_{MIN}$ ). When the analog voltage on the PWM pin is lower than the minimum-operation duty-cycle percentage but higher than the zero-speed analog voltage ( $V_{ANA\_ZS}$ ), the output is controlled by the minimum-operation duty cycle. When the analog voltage on the PWM pin is below zero-speed analog voltage, the DRV10974 enters low-power mode. This is shown in Figure 7-7.



state as the result of a lock condition, the DRV10974 device attempts to restart the motor after  $t_{(LOCK\_OFF)}$  seconds.

The DRV10974 device has a comprehensive lock-detect function that includes six different lock-detect schemes. Each of these schemes detects a particular condition of the lock as shown in [Figure 7-8](#).



**Figure 7-8. Lock Detect**

The following sections describe each lock-detect scheme.

#### **7.3.4.1 Lock Kt Measure**

The DRV10974 device measures the actual Kt of the motor when transitioning from open-loop acceleration to closed-loop acceleration. If the measured Kt is less than 200 mV, the device indicates that the handoff Kt level was not properly reached and the lock is triggered.

#### **7.3.4.2 Lock No Motor**

The phase-U current is checked at the end of the align state. If the phase-U current is not greater than 50 mA, then the motor is not connected. This condition is reported as a lock condition.

#### **7.3.4.3 Lock Open Loop Abnormal**

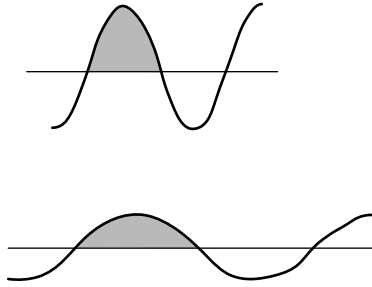
Transition from open loop to closed loop is based on the estimated value of BEMF. If during open-loop acceleration the electrical commutation rate exceeds 200 Hz without reaching the handoff threshold, this lock is triggered.

#### **7.3.4.4 Lock BEMF Abnormal**

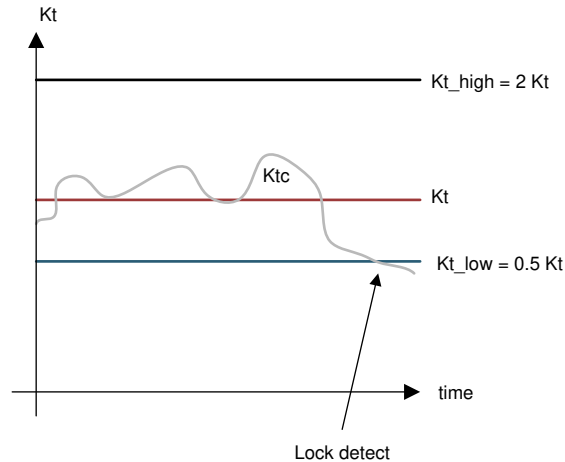
For any specific motor, the integrated value of BEMF during half of an electrical cycle is a constant as shown by the shaded gray area in [Figure 7-9](#). This value is constant regardless of whether the motor runs fast or slow. The DRV10974 device monitors this value and uses it as a criterion to determine if the motor is in a lock condition.

The DRV10974 device uses the integrated BEMF to determine the Kt value of the motor during the initial motor start. Based on this measurement, a range of acceptable Kt values is established. Then, during closed-loop motor operation the Ktc (Kt calculated) value is continuously updated. Finally, the Ktc value is checked to see if it is within the range between  $\frac{1}{2} Kt$  and  $2Kt$ . If the Ktc value goes beyond the acceptable range, a lock condition is triggered as shown in [Figure 7-10](#). Note, there is a blanking period of 0.3 s after the transition from open loop to closed loop where the abnormal BEMF lock is momentarily disabled. The device uses this time to finalize the Kt value that Ktc is compared against.





**Figure 7-9. BEMF Integration**



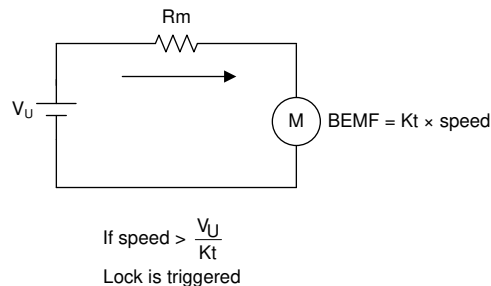
**Figure 7-10. Abnormal Kt Lock Detect**

#### 7.3.4.5 Lock Closed Loop Abnormal

This lock condition is active when the DRV10974 device is operating in the closed-loop mode. The motor is indicated as not moving when the closed-loop commutation period becomes lower than half the previous commutation period. This condition triggers the closed-loop abnormal-lock condition.

#### 7.3.4.6 Lock Speed Abnormal

If the motor is in normal operation, the motor BEMF is always less than the voltage applied to the phase. The sensorless-control algorithm of the DRV10974 device is continuously updating the value of the motor BEMF based on the speed of the motor and the motor Kt as shown in Figure 7-11. If the calculated value for motor BEMF is 1.5 times higher than the applied voltage on phase U ( $V_U$ ) for an electrical period then an error is present in the system, and the calculated value for motor BEMF is wrong or the motor is out of phase with the commutation logic. When this condition is detected, a lock is triggered.



**Figure 7-11. BEMF Monitoring**



short-circuit condition is improved. This function is intended to protect the device and the motor from catastrophic failure when subjected to a short-circuit condition.

### 7.3.7 Overtemperature Protection

The DRV10974 device has a thermal shutdown function which disables the motor operation when the device junction temperature has exceeded the  $T_{SD}$  temperature. Motor operation resumes when the junction temperature becomes lower than  $T_{SD} - T_{SD(hys)}$ .

### 7.3.8 Undervoltage Protection

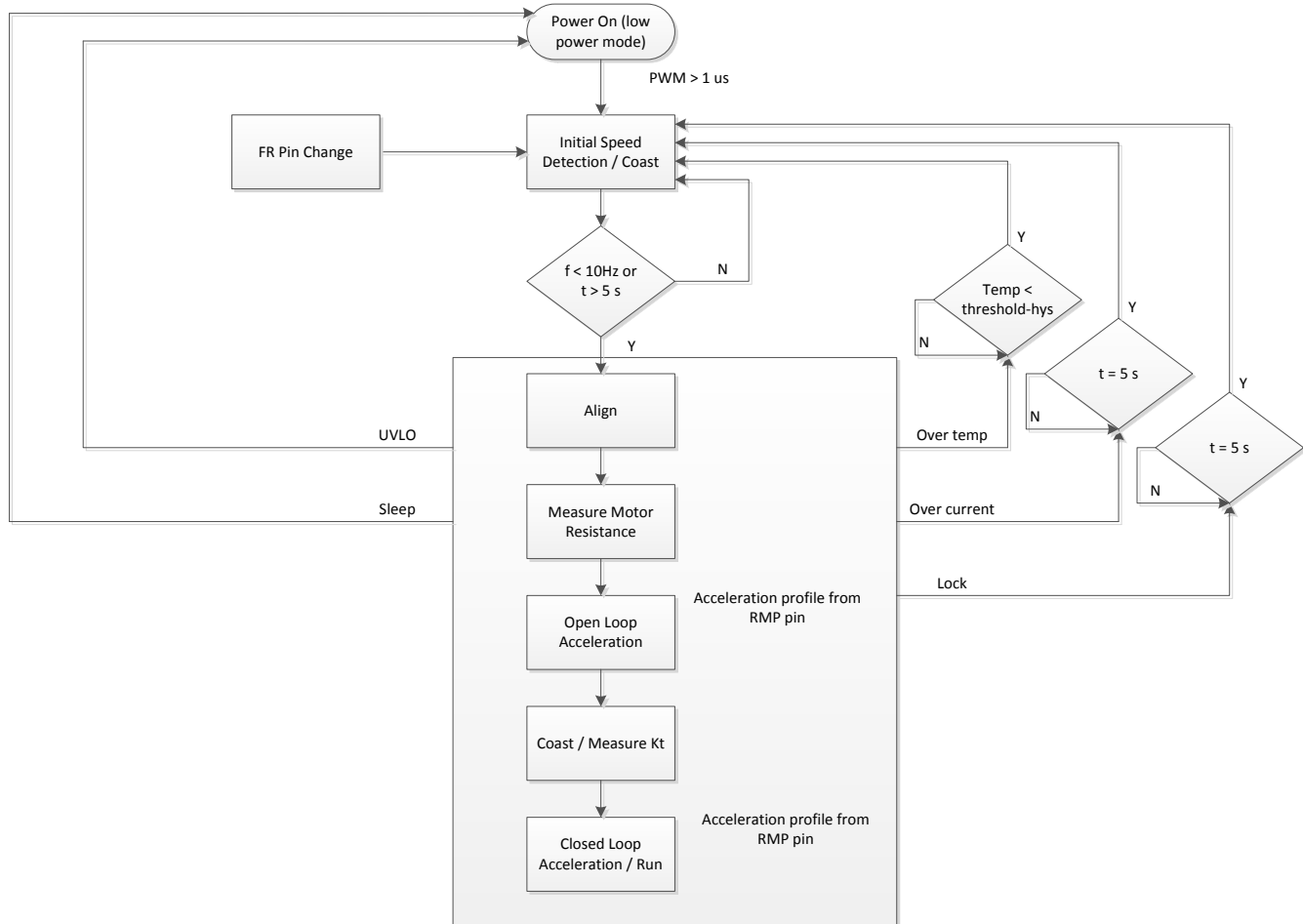
The DRV10974 device has an undervoltage lockout feature, which prevents motor operation whenever the supply voltage ( $V_{CC}$ ) becomes too low. Upon power up, the DRV10974 device operates when  $V_{CC}$  rises above  $V_{(UVLO\_F)} + V_{hys(UVLO)}$ . The DRV10974 device continues to operate until  $V_{CC}$  falls below  $V_{(UVLO\_F)}$ .

## 7.4 Device Functional Modes

### 7.4.1 Spin-Up Settings

#### 7.4.1.1 Motor Start

The DRV10974 device starts the motor using a procedure which is shown in [Figure 7-13](#).



**Figure 7-13. DRV10974 Initialization and Motor Start-Up Sequence**

#### 7.4.1.2 Initial Speed Detect

Every time the DRV10974 device exits low-power mode, it determines if the motor is spinning using a function called initial speed detect. If the frequency on the FG pin is less than 10 Hz, the motor is considered stationary.

If the frequency is greater than 10 Hz the motor is decelerated until it is below 10 Hz or a 5-second time-out has occurred.

### 7.4.1.3 Align

To align the rotor to the commutation logic, the DRV10974 device applies a current equivalent to the closed-loop run current to phase U by driving phases V and W equally. This condition is maintained for a maximum of 0.67 s ( $t_{ALIGN}$ ). To avoid a sudden change in current that could result in undesirable acoustics, the voltage applied to the motor is changed gradually to obtain a current change of 12 A/s.

### 7.4.2 Open-Loop Acceleration

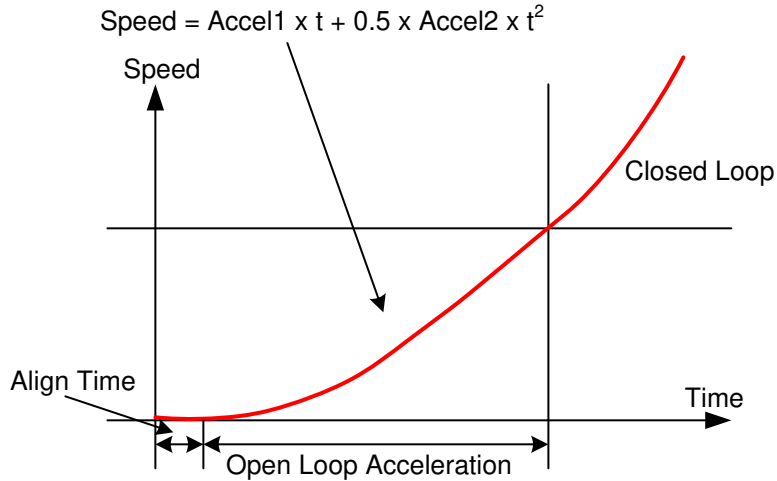
After the motor is confirmed to be stationary and after completing the motor initialization, the DRV10974 device begins to accelerate the motor. This acceleration is accomplished by applying a voltage to the motor at the appropriate drive state and increasing the rate of commutation without regard to the actual position of the motor (referred to as *open-loop operation*). The function of the open-loop operation is to drive the motor to a minimum speed so that the motor generates sufficient BEMF to allow the commutation control logic to drive the motor accurately.

The motor start-up profile can be configured using an external resistor to set the acceleration profile before transitioning to closed-loop operation. [Figure 7-14](#) shows this acceleration profile. During closed-loop operation the RMP pin controls the closed-loop acceleration and deceleration. [Table 7-2](#) lists the selectable acceleration parameters.

**Table 7-2. Acceleration Profile Settings**

RMP SELECTION	$R_{RMP}$ [k $\Omega$ ] <sup>(1)</sup>	Accel2 [Hz/s <sup>2</sup> ]	Accel1 [Hz/s]	CLOSED-LOOP-ACCELERATION TRANSITION TIME [s] <sup>(2)</sup>	CLOSED-LOOP-DECELERATION TRANSITION TIME [s] <sup>(3)</sup>
0	7.32	0.22	4.6	2.7	44
1	10.7	1.65	9.2	2.7	22
2	14.3	1.65	15	1	22
3	17.8	3.3	25	1	11
4	22.1	7	25	0.2	44
5	28	7	35	0.2	22
6	34	14	50	0.2	22
7	41.2	27	75	0.2	11
8	49.9	27	75	5.4	11
9	59	14	50	8	22
10	71.5	7	35	11	22
11	86.6	7	25	22	44
12	105	3.3	25	5.4	11
13	124	1.65	15	8	22
14	150	1.65	9.2	11	22
15	182	0.22	4.6	22	44

- (1) All resistors are  $\pm 1\%$
- (2) Time to transition from 0 to 100% duty cycle.
- (3) Time to transition from 100% to 0% duty cycle.



**Figure 7-14. Start-Up Profile**

### 7.4.3 Start-Up Current Sensing

The start-up peak current is controlled by the current-sense limit resistor,  $R_{(CS)}$ . The start current is set by selecting the  $R_{(CS)}$  resistor based on [Table 7-3](#). The current should be selected to allow the motor to accelerate reliably to the handoff threshold. Heavier loads may require a higher current setting, but the rate of acceleration is limited by the selected resistor,  $R_{(RMP)}$ .

**Table 7-3. Start-Up Current Limit**

$R_{(CS)}$ [k $\Omega$ ] <sup>(1)</sup>	$I_{(LIMIT)}$ [mA]
7.32	200
16.2	400
25.5	600
38.3	800
54.9	1000
80.6	1200
115	1400
182	1600 (1500 for align)

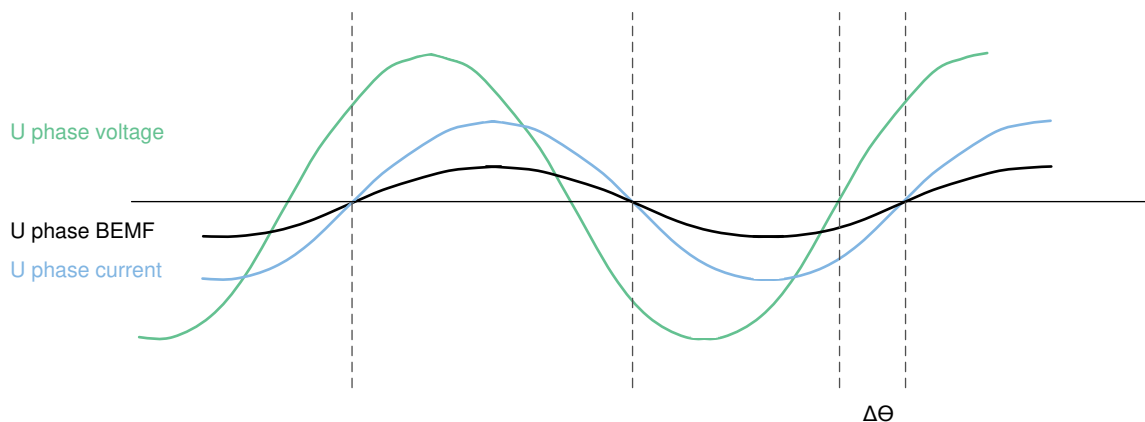
(1) All resistors are  $\pm 1\%$ .

#### 7.4.4 Closed Loop

When the motor accelerates to the target BEMF threshold, commutation control transitions from open-loop mode to closed-loop mode. During this transition, the motor is allowed to coast for one electrical cycle to measure  $K_t$ . The commutation drive sequence and timing are determined by the internal control algorithm, and the applied voltage is determined by the PWM-commanded duty-cycle input. The closed-loop acceleration and deceleration values are provided in [Table 7-2](#).

#### 7.4.5 Control Advance Angle

To achieve the best efficiency, the drive state of the motor must be controlled such that the current is aligned with the BEMF voltage of the motor. [Figure 7-15](#) illustrates the operation when the drive angle has been optimized. For complete flexibility, the DRV10974 device offers a wide range of fixed lead times. The options for lead time are controlled by a resistor on the ADV pin. The values available are shown in [Table 7-4](#).

**Figure 7-15. Drive Angle Adjustment**

**Table 7-4. Lead Time Selection**

$R_{ADV}$ [k $\Omega$ ] <sup>(1)</sup>	LEAD TIME [ $\mu$ s]
10.7	10
14.3	25
17.8	50
22.1	100
28	150
34	200
41.2	250
49.9	300
59	400
71.5	500
86.6	600
105	700
124	800
150	900
182	1000

(1) All resistors are  $\pm 1\%$ .

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DRV10974 device is used in sensorless 3-phase BLDC motor control. The driver provides a high-performance, high-reliability, flexible, and simple solution for appliance fan, pump, and blower applications. The following design shows a common application of the DRV10974 device.

### 8.2 Typical Application

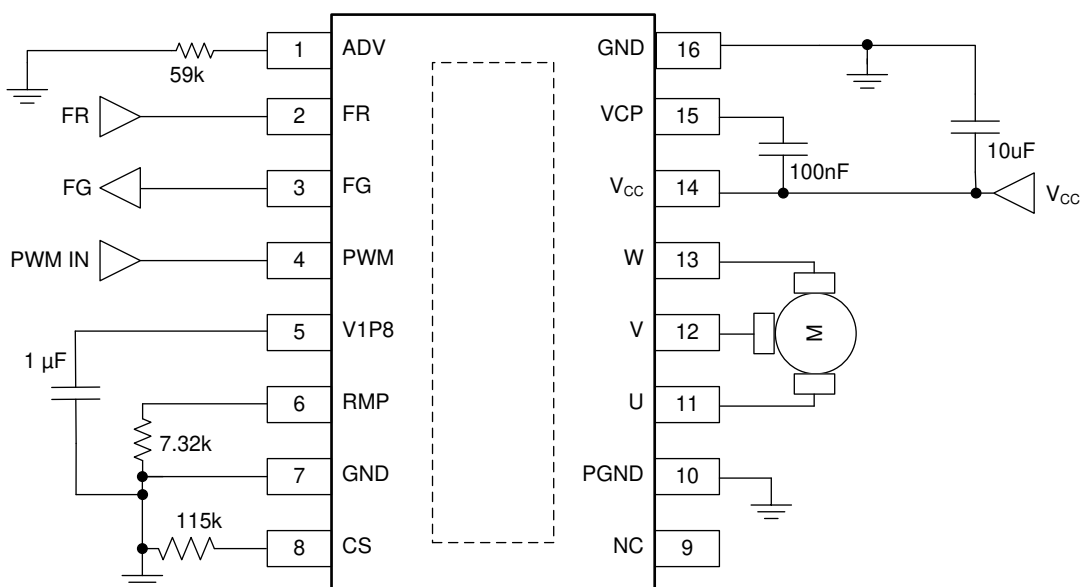


Figure 8-1. Typical Application Schematic

Table 8-1. Recommended External Components

NODE 1	NODE 2	COMPONENT
V <sub>CC</sub>	GND	10-µF, 25-V ceramic capacitor tied from V <sub>CC</sub> to ground
VCP	V <sub>CC</sub>	100-nF, 10-V ceramic capacitor tied from VCP to V <sub>CC</sub>
V1P8	GND	1-µF ±30%, 6.3-V ceramic capacitor tied from V1P8 to ground
RMP	GND	1%, 1/8-watt resistor tied from RMP to ground to set the desired acceleration profile
CS	GND	1%, 1/8-watt resistor tied from CS to ground to set the desired current limit
ADV	GND	1%, 1/8-watt resistor tied from ADV to ground to set the desired lead angle (time)





## 9 Power Supply Recommendations

The DRV10974 device is designed to operate from an input voltage supply,  $V_{CC}$ , range between 4.4 V and 18 V. The user must place a minimum of a 10- $\mu$ F capacitor rated for  $V_{CC}$  between the  $V_{CC}$  and GND pins and as close as possible to the  $V_{CC}$  and GND pins.

If the power supply ripple is more than 200 mV, in addition to the local decoupling capacitors, a bulk capacitance is required and must be sized according to the application requirements.

## 10 Layout

### 10.1 Layout Guidelines

- Use thick traces when routing to the  $V_{CC}$ , GND, U, V, and W pins, because high current passes through these traces.
- Place the 10- $\mu\text{F}$  capacitor between  $V_{CC}$  and GND, and as close to the  $V_{CC}$  and GND pins as possible.
- Place the 100-nF capacitor between VCP and  $V_{CC}$ , and as close to the VCP and  $V_{CC}$  pins as possible.
- Connect GND and PGND under the thermal pad.
- Keep the thermal pad connection as large as possible. It should be one piece of copper without any gaps.

### 10.2 Layout Example

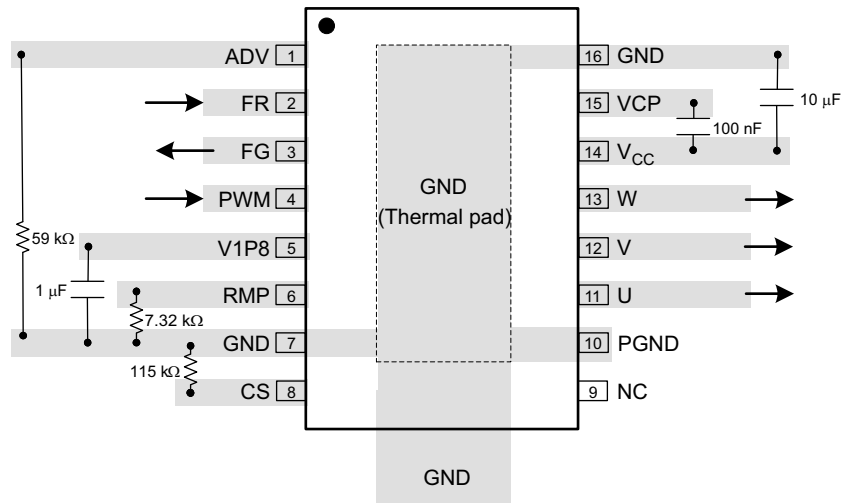


Figure 10-1. HTSSOP Layout Example

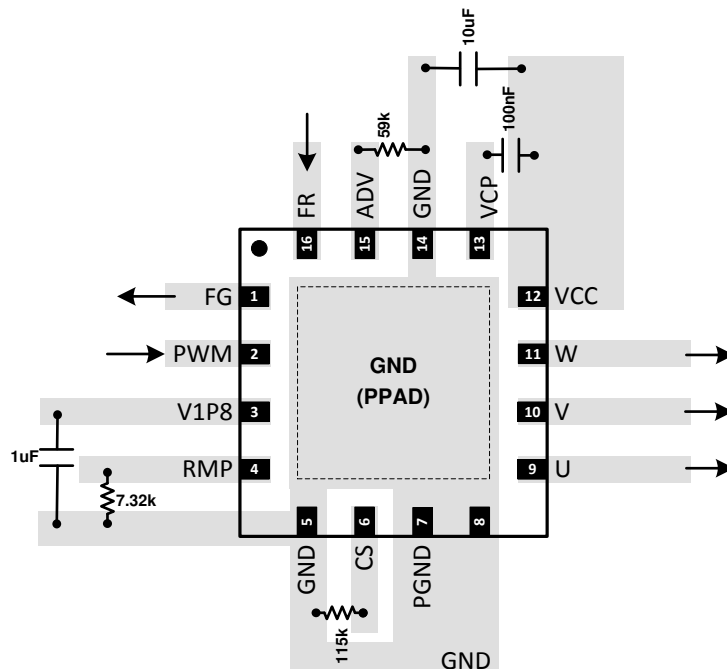


Figure 10-2. QFN Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV10974PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	10974	
DRV10974RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 10974	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

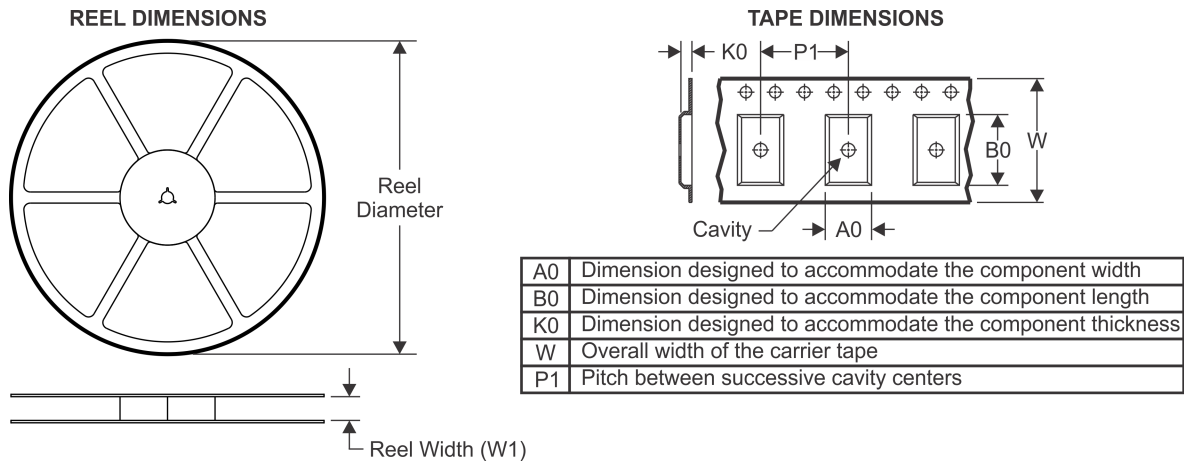
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION

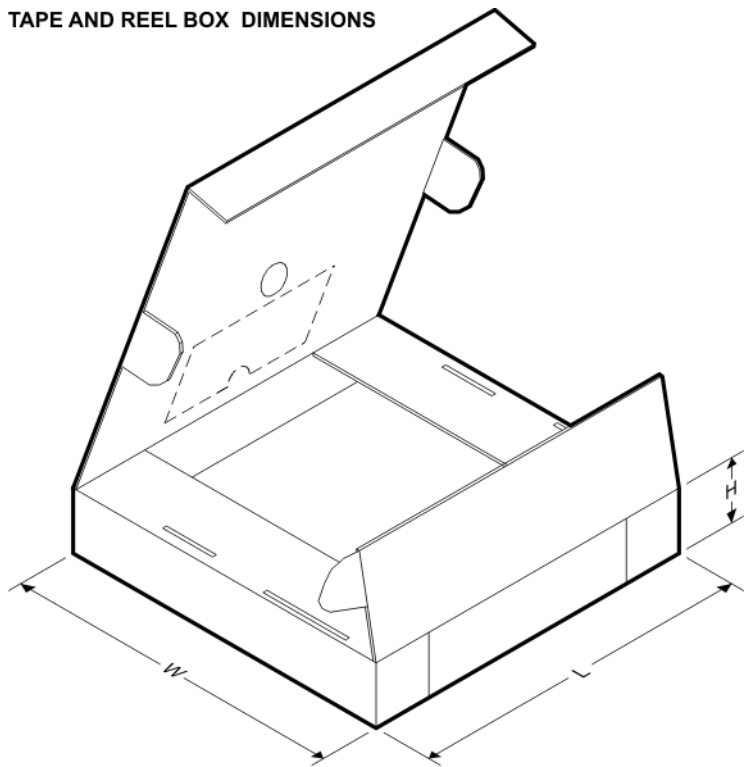


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

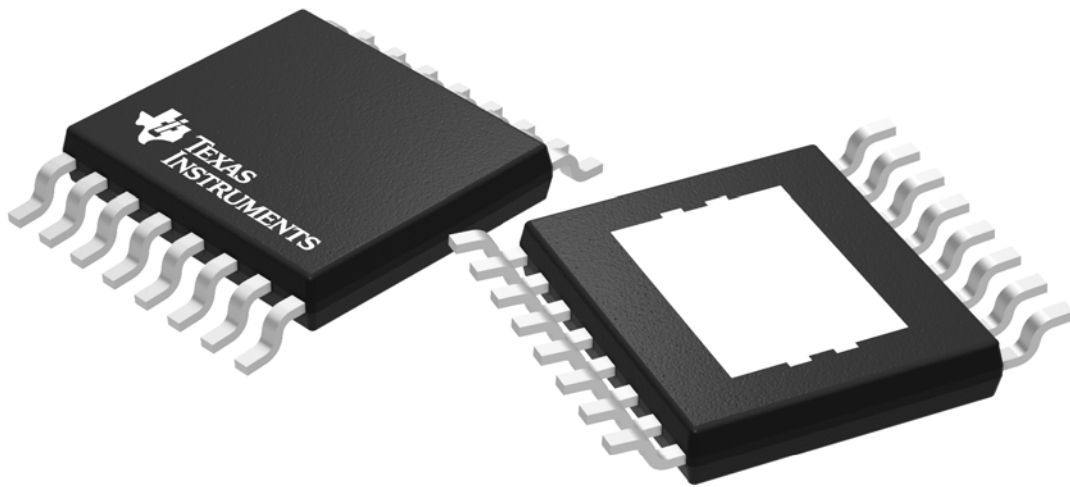
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV10974PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV10974RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

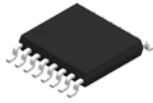
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV10974PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
DRV10974RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0





Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

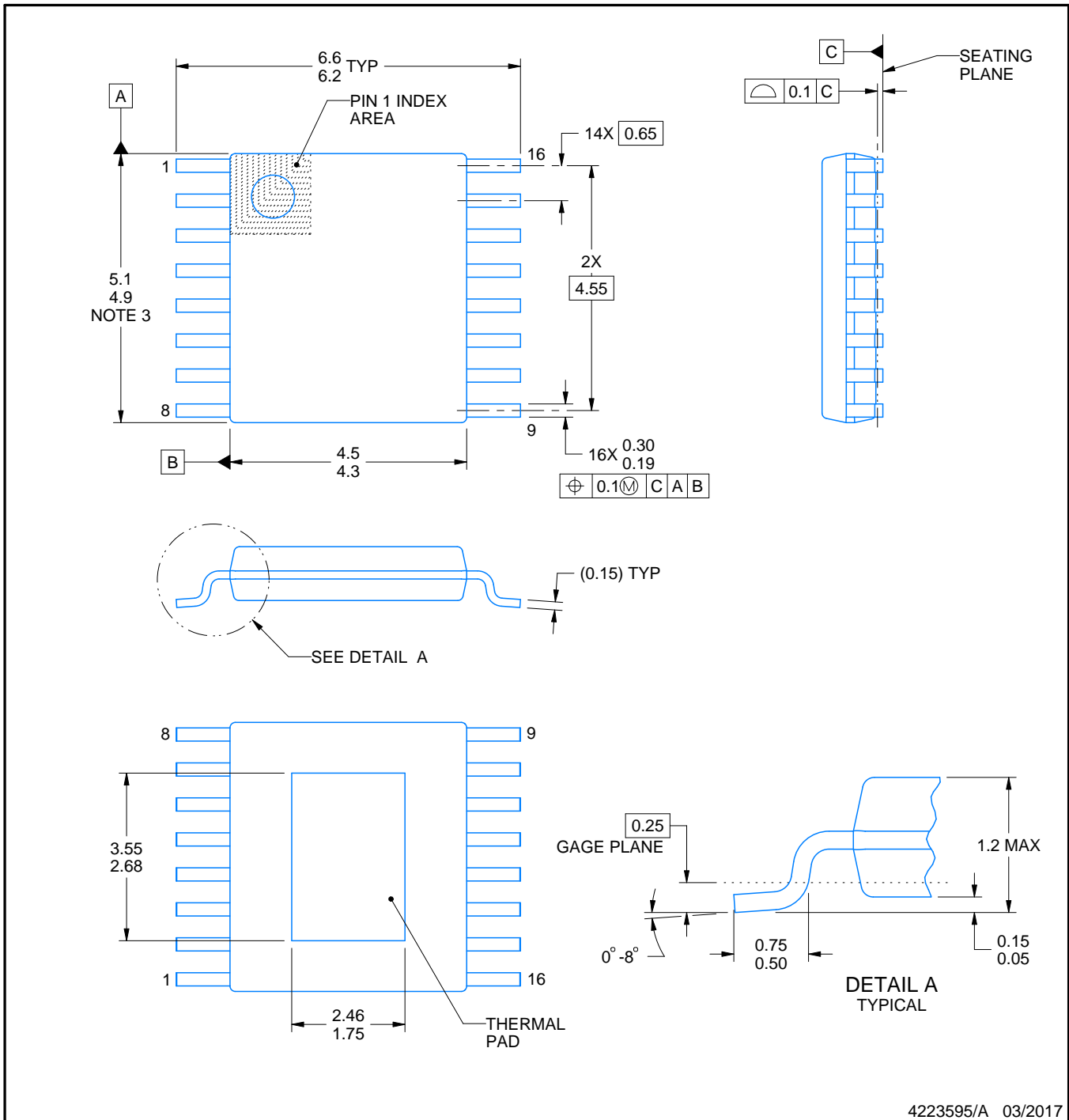
PWP0016J



# PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

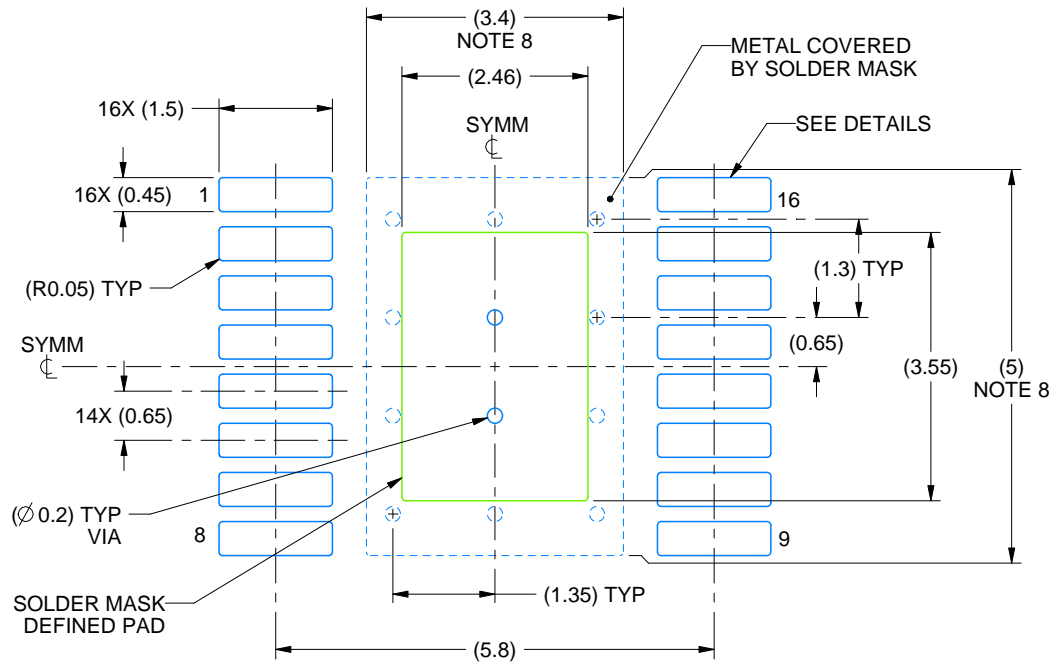
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

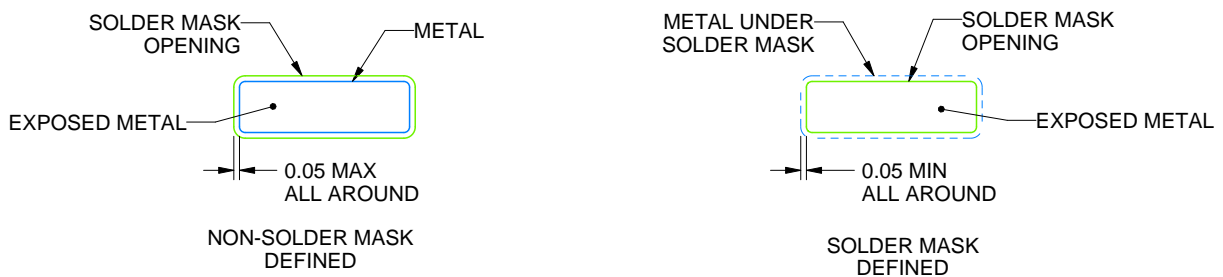
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

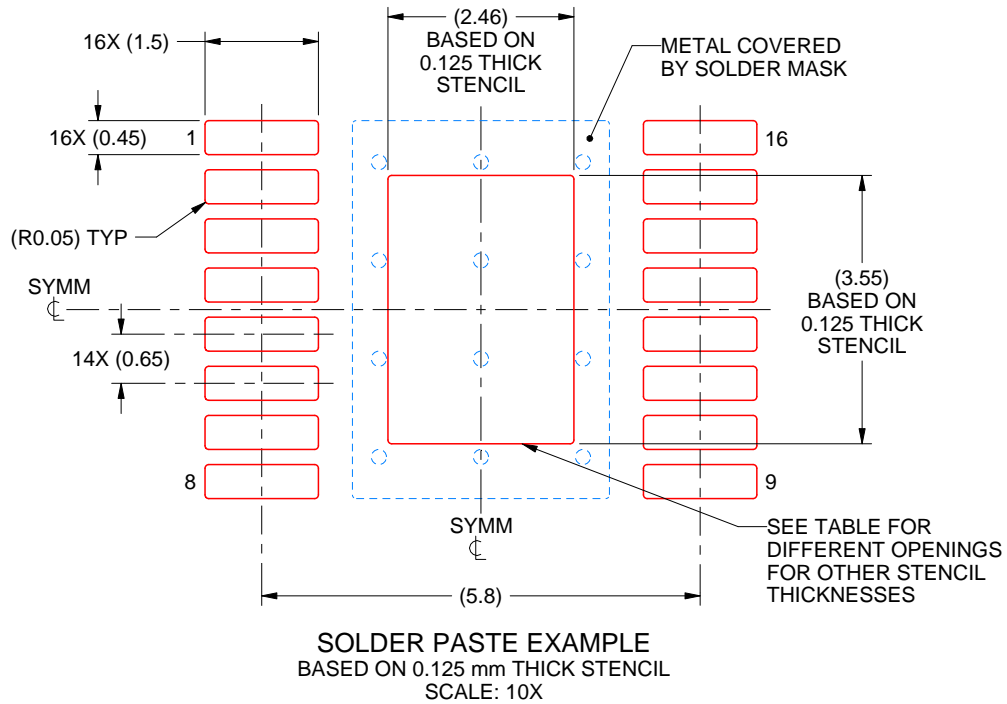
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

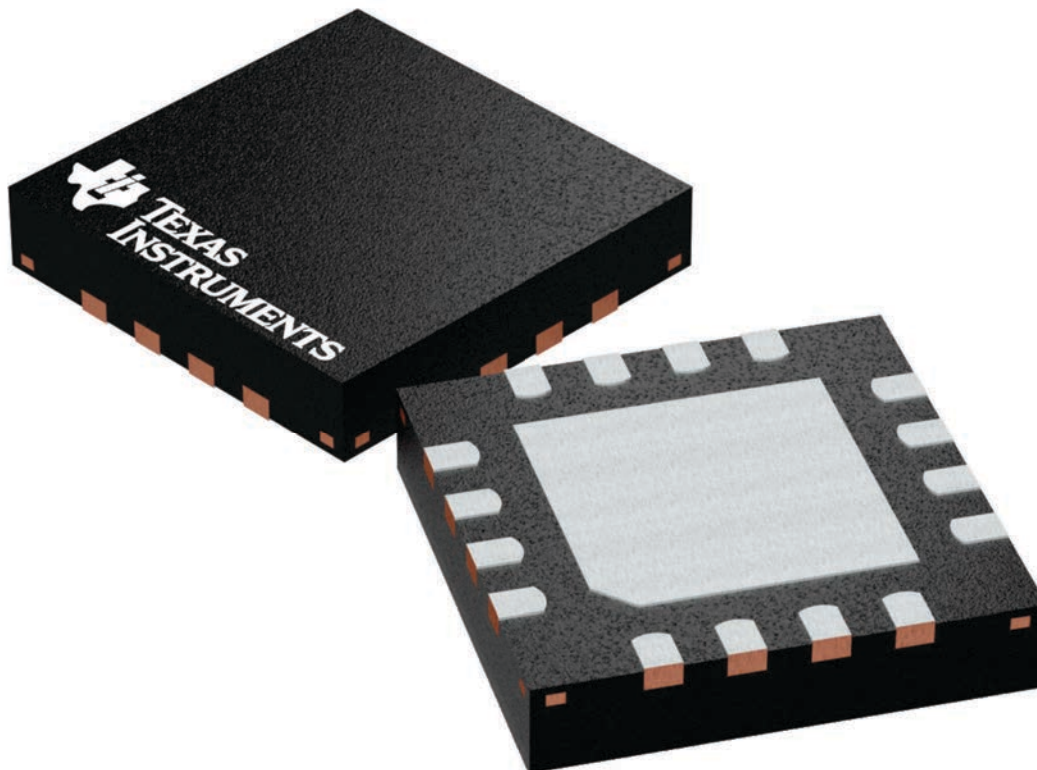
**RUM 16**

**WQFN - 0.8 mm max height**

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

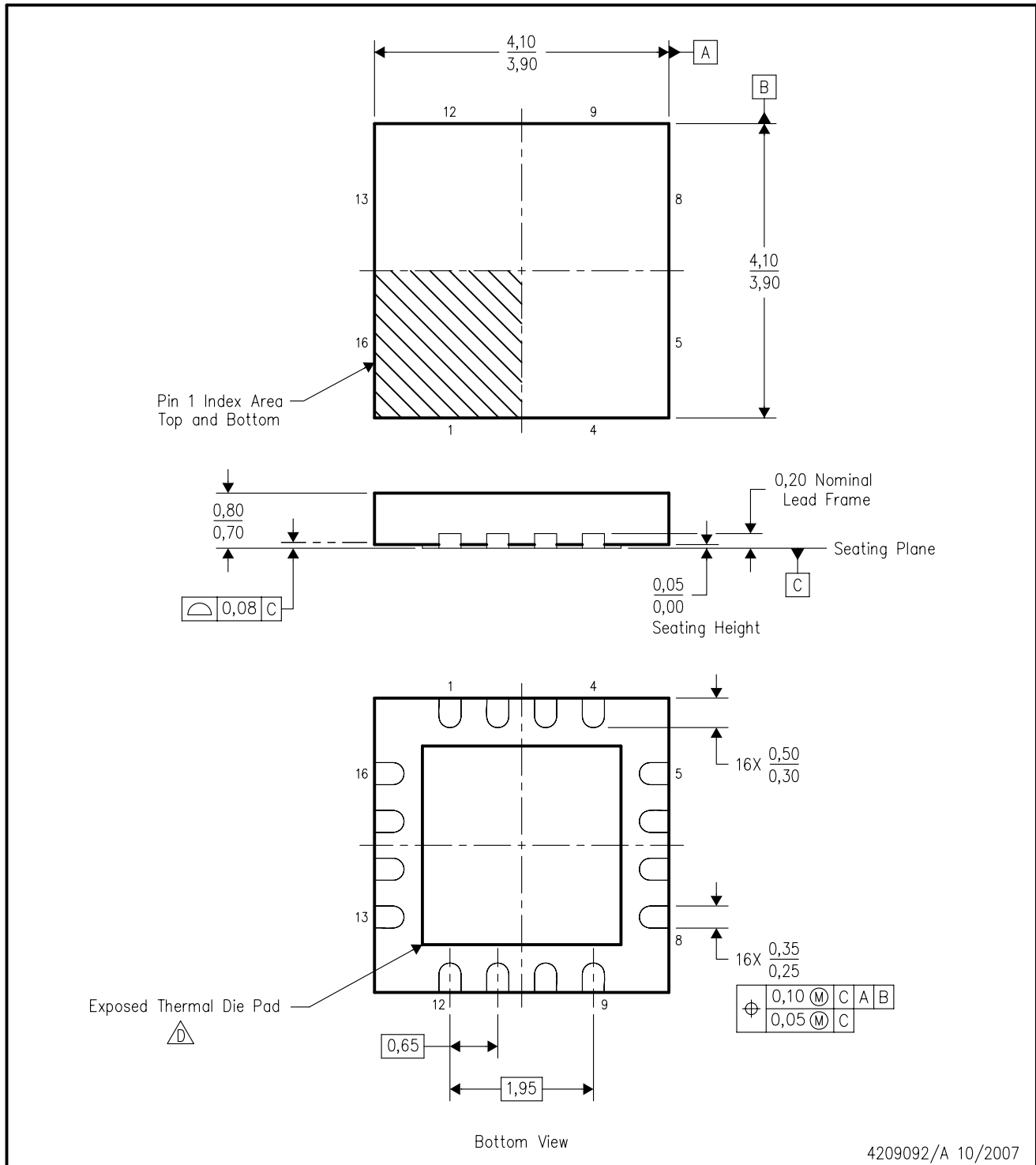
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.




4224843/A

RUM (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4209092/A 10/2007

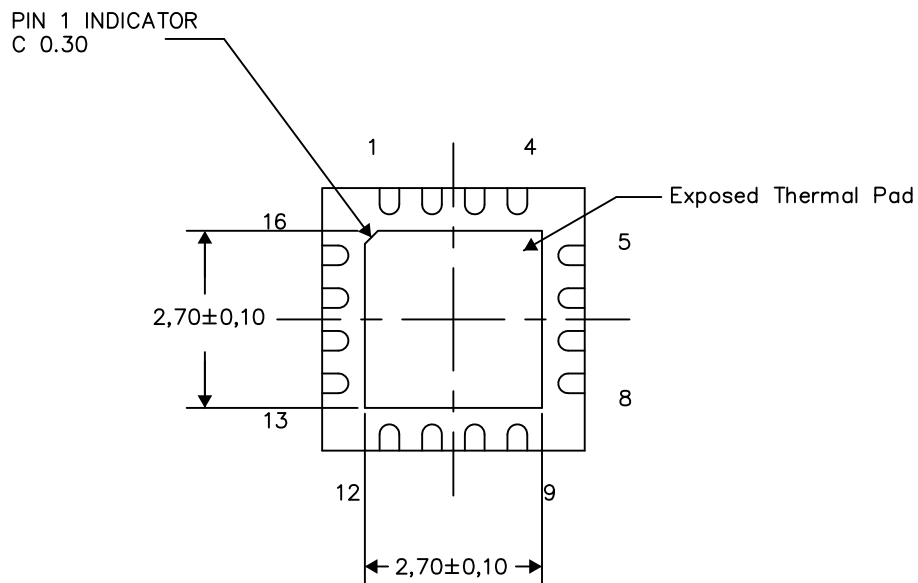
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-220 variation WGGC-3.

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209093-2/F 09/15

NOTES: All linear dimensions are in millimeters





## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated